

Gennum's Snowbush IP Group Delivers the Industry's First PCI Express 3.0 PHY IP on TSMC 40nm Process

PCIe 3.0 PHY and Controller Provide Complete IP Solution for Improving Time-to-Market and Reducing Integration Risk

Burlington, Ontario, June 8, 2009 – Leveraging its high-speed serial interface and digital systems expertise, Gennum Corporation (TSX: GND) today announced that its Snowbush IP group has developed the industry's first available integrated PCI Express® 3.0 (Gen 3) PHY and Controller IP solution. The new PCIe® 3.0 cores can be licensed immediately by system-on-a-chip (SoC) and system companies, enabling early deployment of PCIe 3.0 (Gen 3) in systems requiring the 8.0 Gigatransfers per second (GT/s) performance of this new PCI-SIG standard. PCIe 3.0 opens up more bandwidth using the same physical connectors and adds new features to improve the user experience in server network and computer products using PCI Express.

“PCIe 3.0 IP is critical for the development of next-generation computing products. Our momentum in high-speed IP is unquestionable with our recent SATA 6.0 Gb/s IP release, and now our customers can license our 8 GT/s PCI-Express IP. Snowbush IP again demonstrates it consistently delivers silicon-proven cores at the leading edge of another emerging market, enabling many high-profile semiconductor suppliers and OEMs to get to market first,” said Ewald Liess, General Manager of the Snowbush IP group for Gennum. “Our customers rely on our extensive experience at data rates of 5 Gb/s and above—high-speed serial interface IP that is high yielding and optimized for the performance, power, size, and cost of our customers' target applications. They know and see the value of outsourcing these complex IP blocks.”

“PCI Express 3.0 doubles the effective throughput of the existing 2.0 standard, meeting many of the future throughput needs of interface chips for servers, communications, and enterprise storage devices,” said Jag Bolaria, senior analyst at the Linley Group. “We anticipate that this new standard will begin to see deployment in 2010. Snowbush now has both the PHY and Controller, allowing PCIe 3.0 market movers a cost-effective way to deploy products based on this standard.”

Delivering Next-Generation PCIe Solutions for Rapid Time to Market

The new Snowbush PCIe 3.0 IP is architected for low power and area on both the PHY and Data Link layer, and features low power consumption from a proprietary 5-tap Decision Feedback Equalization (DFE) and H-bridge transmit driver. The PHY silicon footprint is small and includes the I/Os, ESD structures, and PCS Layer, in 1-, 2-, 3-, and 4-lane configurations to reduce silicon cost. Each lane of the PHY can be configured to operate in Gen 1, Gen 2, or Gen 3

mode. Multiple 4-lane PHYs can be configured as x8, x16, x32, and greater links. An on-chip Fractional-N PLL Frequency Synthesizer with integrated Spread Spectrum Clocking is used for simplified external clocking and reduced SoC complexity.

The Controller features a low latency pipelined architecture that achieves industry-leading throughput. Available as an Endpoint, Root, Dual Mode, and Switch for x1, x4, x8, and x16 lane configurations the digital controller can be targeted for any application of PCI Express. The Controller's micro and macro power options deliver a low energy profile that compliments the PHY layer's low power consumption, together providing industry-leading thin power characteristics for mobile-based SoCs requiring PCI Express.

Snowbush IP Core Enables Early Adoption of PCIe 3.0

The integrated Snowbush device PHY and Controller solution satisfies the 8 GT/s speed requirement of PCIe 3.0, and exceeds the anticipated critical specifications for jitter performance over harsh channels on the PHY side. Low latency and power requirements in the link layer provide substantial margin to designers for creating robust products with excellent interoperability.

The new Snowbush PHY IP block employs a variety of techniques to ensure superior performance, reduced jitter and maximum noise immunity, including:

- A proprietary dual-loop hybrid clock-and-data recovery (CDR) architecture which recovers the clock with less jitter
- A coupled ring oscillator VCO design with jitter performance usually only found in complex LC tank oscillators
- Internal voltage and current regulation for sensitive circuits
- Fully differential circuitry and clock signaling
- Extensive use of guard rings within the macro

The new Controller IP block features:

- Atomic Operation (FetchAdd, Swap, Compare and Swap (CAS))
- Address translation services
- Transaction-Layer Processing Hints (TPH)
- 5.0 GT/s and 8.0 GT/s speed negotiation
- Optional and Mandatory Power Management Features

The new cores join a full suite of high-speed IP solutions that currently include PHY and controller products supporting the PCI Express 1.x, and 2.0, Serial ATA (SATA) 1.5 Gb/s, 3.0 Gb/s and 6.0 Gb/s, Fibre Channel and other high-speed standards requiring data rates from 5 Gb/s to 10 Gb/s data rates and beyond.

The new IP is supported by a team of specialized interconnect experts focused on the development of high-speed interface IP with a proven track record of ensuring right-the-first-time silicon for customers.

Pricing and Availability

The Snowbush integrated [PHY and Controller](#) PCIe 3.0 IP is available immediately for licensing in TSMC 40nm and below, and can be ported to other leading foundries. The Link Layer controller should be available for early code drop by November 2009. For more information on licensing terms and pricing, please contact sales@snowbush.com. For more information on the PCIe 3.0 IP solution from Gennum's Snowbush IP group visit www.snowbush.com/pcie3.

About the Gennum Snowbush IP Group

The Gennum Snowbush IP group offers a team of interconnect specialists to design and deliver silicon-proven, high-speed serial interface IP. Comprising one of the industry's most robust, widely-deployed, production-tested and customizable family of IP cores, the Snowbush IP portfolio satisfies the needs of today's most demanding high-speed serial communication protocols and applications. Snowbush IP offers integrated PHY and Controller solutions for standards like USB, PCI Express[®] and Serial ATA (SATA), and single and multi-standard SerDes for applications with data rates from 1 Gb/s to over 10 Gb/s. Gennum's Snowbush IP group is committed to supporting customers with diverse foundry and process requirements, offering IP cores for TSMC, UMC, Common Platform, and Fujitsu processes. For more information visit www.snowbush.com.

About Gennum

Gennum Corporation (TSX: GND) designs innovative semiconductor solutions and intellectual property (IP) cores for the world's most advanced consumer connectivity, enterprise, video broadcast and data communications products. Leveraging the company's proven optical, analog and mixed-signal products, and IP, Gennum enables multimedia and data communications products to send and receive information without compromising the signal integrity. A recognized award-winner for advances in high definition (HD) broadcasting, Gennum is headquartered in Burlington, Canada, and has global design, research and development and sales offices in Canada, Germany, India, Japan, Korea, Mexico, Taiwan, the United States and the United Kingdom.

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