



## HIGHLIGHTS

- Targeted for high-resolution, high-speed data conversion applications such as ultra wide-band and next-generation wireless networking
- Greater than 10.5-bit ENOB at 1Gsp/s
- Serial data transmission (quad 5Gs/s)
- Backed by a commitment to integration and customization support, if required
- Available Q2 2008

## TECHNOLOGY

- Designed in TSMC 90G 1.0V and 1.8V standard digital process
- Uses 6 layers of metal
- Supports flip-chip or QFP packaging
- Utilizes 1.0V thin-oxide and 1.8V thick-oxide devices

## FEATURES

- Four time-interleaved 14bits pipeline ADC each operating at 250Ms/s
- Auto gain/offset/skew adjustment
- Better than 2-LSB DNL and 4-LSB INL performance
- Integrated with the SNOWBUSH SBPHY2000T90G to serially transmit ADC output with a quad semi PCIe
- Accessible register controls allow user-specific optimization of critical ADC parameters (e.g. power-consumption, gain, offset)
- Includes saturation indicator outputs for use with automatic gain control circuitry
- On-chip LDO regulators increase noise immunity to power-supply and substrate noise
- Can be used as four single 14bit ADCs at 250MS/s

Parameter	Min	Typ	Max	Unit
<b>ADC Functional Specifications</b>				
Sampling Frequency		1		GHz
ADC Resolution		14		Bits
Output Data Bus Width		4		Bits @ 5 GSPS
Power @ 1V/2.5V			1	W
Area*		10		mm <sup>2</sup>
<b>ADC Sampling Clock Specifications</b>				
Sampling Clock RMS Jitter			2ps	ps
Sampling Clock Duty-Cycle	45		55	%
<b>ADC Electrical Specifications</b>				
ADC Input Common-Mode Voltage	0.6		0.9	V
ADC Input Differential Voltage		1.2		V <sub>DIFF-pk-pk</sub>
ADC Gain Control	100		200	% (digitally programmable)
ADC Gain Matching			0.5	dB
ADC Offset Matching			8	LSB
Differential Non-Linearity			2	LSB
Integral Non-Linearity			4	LSB
ENOB	10.5			Bits
SFDR	68	75		dBc

\* Excludes bias circuit area

## TEST FEATURES

A wide range of powerful production and prototype test features are included:

- Diagnostics capability via internal digital calibration circuitry
- Devoted analog test pads allows for analog coverage during production testing
- Integrated test circuitry allows for complete characterization within production parts

## DELIVERABLES

The SNOWBUSH 14-bit, 1Gsp/s ADC is delivered as a GDSII hard macro. Standard deliverables include:

- Detailed Specification and Integration Guide
- LEF abstract
- GDSII layout and mapping files
- HSpice compatible netlist for LVS
- Verilog model
- Liberty timing model for STA

## SNOWBUSH IP Cores

SNOWBUSH offers a wide-range of additional silicon proven, mixed-signal IP Cores:

- PCIe™/SATA PHYs
- Low-Jitter PLLs
- Frequency Synthesizers
- Video/Graphics cores

Every time you choose SNOWBUSH IP cores you receive:

- Reliable, high-performance IP cores developed under a rigorous mixed-signal verification and validation methodology
- The ability to customize IP features to meet specific application needs
- Value added custom services such as layout, test and characterization capabilities

For more information about this product or other SNOWBUSH services please email us at [sales@snowbush.com](mailto:sales@snowbush.com) or call +1-416-925-5643.

